A NOVEL DEPOSITION METHOD FOR Si-Ge EPI LAYER ON DIFFERENT INTERMEDIATE SUBSTRATES

FIELD OF THE INVENTION

The present invention relates generally to semiconductor fabrication and more specifically to semiconductor transistor fabrication.

BACKGROUND OF THE INVENTION

Silicon-germanium epitaxial (Si-Ge epi) technology is becoming the mainstream in the application of heterojunction bipolar transistors. Si-Ge epi layers are used as the base material in such transistors in BiCMOS applications where bi-polar (BI) and complementary metal-oxide semiconductor (CMOS) transistors are fabricated in different areas of the same wafer. The Si-Ge epi layer could provide higher emitter injection efficiency and lower base transit time.

However, the discontinuity of the Si-Ge epi layer occurs on different intermediate layers and becomes a major issue for subsequent process steps due to poor polysilicon (poly) sheet resistance connected with the base electrode.

U.S. Patent No. 6,388,307 B1 to Kondo et al. describes a B-doped SiGe layer in a transistor process.

U.S. Patent No. 5,976,941 to Boles et al. describes a SiGe epi process.

U.S. Patent No. 5,273,930 to Steele et al. describes a SiGe epi process on a silicon seed layer.

U.S. Patent No. 5,620,907 to Jalali-Farahani et al. describes a method for a heterojunction bipolar transistor.

SUMMARY OF THE INVENTION

Accordingly, it is an object of one or more embodiments of the present invention to provide a method of fabricating semiconductor transistors utilizing Si-Ge epi layers.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure is provided and a doped Si-Ge seed layer is formed thereover. The doped Si-Ge seed layer having increased nucleation sites. A Si-Ge epitaxial layer upon the doped Si-Ge seed layer whereby the Si-Ge epitaxial layer lacks discontinuity.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 3 schematically illustrates a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Initial Structure - Fig. 1

As shown in Fig. 1, structure 10 has a seed layer 12 formed thereover. Structure 10 is preferably an intermediate substrate and may be a silicon substrate and is understood to possibly include a semiconductor wafer or substrate, active and passive devices formed within the wafer, conductive layers and dielectric layers (e.g., inter-poly oxide (IPO), intermetal dielectric (IMD), etc.) formed over the wafer surface. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer. Structure 10 may also include silicon oxide and/or polysilicon.

Seed layer 12 is preferably a doped Si-Ge layer having a thickness of preferably from about 10 to 400Å and more preferably from about 20 to 200Å. Doped Si-Ge seed layer 12 is preferably doped with boron (B), C, P or As and is more preferably doped with boron (B).

When doping with boron, B_2H_6 is introduced during the formation of Si-Ge seed layer 12 at a rate of preferably from about 0 to 100 sccm and more preferably from about 0 to 50 sccm under the following conditions:

temperature: preferably from about 500 to 750°C and more preferably from about 600 to 700°C;

pressure: preferably from about 20 to 200 Torr and more preferably from about 50 to 150 Torr; and

time: preferably from about 10 to 120 seconds and more preferably from about 10 to 60 seconds.

The dopant within doped Si-Ge seed layer 12 preferably has a concentration of from about 1E18 to 1E20 atoms/cm^2 and more preferably about 1E19 cm^2.

The addition of a dopant to the Si-Ge forms the doped Si-Ge seed layer 12 permitting much better step coverage and eliminates discontinuity by, the inventors believe, increasing the nucleation sites.

<u>Formation of Si-Ge Epitaxial Layer 14 - Fig. 2</u>

As shown in Fig. 2, a Si-Ge epitaxial (epi) layer 14 is formed upon the doped Si-Ge seed layer 12 to a thickness of preferably from about 100 to 700Å and more preferably from about 200 to 500Å. Si-Ge epi layer 14 is formed under the following conditions:

Si precursor: preferably SiH_4, SiH_2Cl_2, $SiHCl_3$ or $SiCl_4$ and more preferably SiH_4;

Ge precursor: preferably GeH_4 or $GeCl_4$ and more preferably GeH_4;

temperature: preferably from about 500 to 750°C and more preferably from about 600 to 700°C;

pressure: preferably from about 20 to 200 Torr and more preferably from about 50 to 150 Torr; and

time: preferably from about 20 to 400 seconds and more preferably from about 100 to 300 seconds.

The epi layer 14 could have Si-Ge epi film with graded or box Ge profile. The epi film 14 might also have other doping concentrations.

Formation of Optional Cap Layer 16 - Fig. 3

As shown in Fig. 3, a cap layer 16 may be optionally formed over the Si-Ge epitaxial layer 14 to a thickness of preferably from about 20 to 200Å and more preferably from about 40 to 120Å to finish the base process in a BiCMOS process flow.

Due to the doped Si-Ge seed layer, the discontinuity issue is eliminated.

Cap layer 16 is preferably comprised of silicon.

Advantages of the Present Invention

The advantages of one or more embodiments of the present invention include:

1. shorten the incubation time of seed layer;

2.improve film uniformity on different substrates; and

3. improve epi quality.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.